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Final Report

High-Electron Mobility Graphene Channel Transistors for Millimeter-Wave Applications

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***Abstract*—A key findings in the last year's study is hydrogen treatment for surface cleaning of graphene. However resulting FET fabricated using SiN gate stack suffered from low carrier mobility. In this year's study, SiCN deposited by plasma-enhanced chemical vapor deposition (PECVD) using hexamethyldisilazane (HMDS) vapor is studied. During PECVD, hydrogen is used as a carrier gas in addition to HMDS vapor. This becomes an advantage in the graphene process because hydrogen has cleaning effect on graphene surface. To verify this effect, SiCN gate stack is applied to the graphene FETs on SiC substrates. FETs with SiCN gate stack exhibit clearer ambipolar characteristics than FETs with conventional SiN gate stack. The extrinsic transconductance is 35 mS/mm for n-type operation and 33 mS/mm for p-type operation. Corresponding field effect mobility is estimated to be 300 and 280 cm^2/(V.s) for electrons and holes, respectively. The SiCN gate stack is also applied to Graphene-On-Silicon Field-Effect Transistors (GOSFETs).**

I. INTRODUCTION

Graphene is becoming a promising candidate of channel materials in field-effect transistors because of its high carrier mobility both for electrons and holes [1]. Last year we have fabricated FETs employing epitaxial graphene formed on semi-insulating SiC substrates by thermal decomposition approach [2,3]. Resulting device exhibited an extrinsic transconductance of 0.1 mS/mm and an electron mobility of 50 cm^2/(V.s). In order to improve these characteristics, we focus on the gate dielectric stack and its process. This year, a SiCN gate stack is studied for graphene FETs. Using the SiCN gate stack, clear ambipolar characteristics with the conduction minimum at zero gate voltage is confirmed by the graphene FETs on SiC substrates.

Usually the thermal decomposition of SiC is a possible approach if one uses SiC substrates. In 2009, M. Suemitsu *et al.* reported the epitaxial graphene on Si substrates [4,5]. In this approach, a SiC layer is first grown on Si substrates and then the surface of the SiC layer is thermally decomposed to form graphene by annealing at ultrahigh vacuum. We have reported top-gate *graphene-on-silicon* FETs (GOSFETs) using a SiN gate stack [6]. However these devices have issues that the drain current density was very small (in the order of 10^{-3} mA/mm) and a deep negative shift in the Dirac voltage (~ -60 V) was observed. In this work, the SiCN gate stack is also applied to GOSFETs. The drain current density increases by two orders of magnitude comparing to the previous GOSFETs [6] using the SiN gate stack.

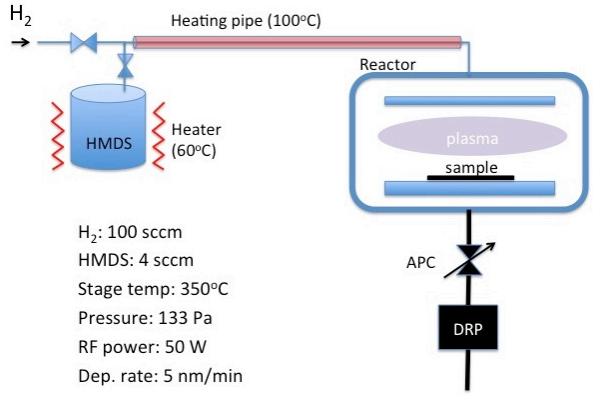

Figure 1. Diagram of PECVD system. Liquid HMDS is heated at 60°C. Vaporized HMDS is introduced into the reactor through the heated pipe. Hydrogen is also introduced into the reactor as a carrier gas. The working pressure is controlled by the automatic pressure controller (APC) and the dry vacuum pump (DRP).

II. FORMATION OF EPITAXIAL GRAPHENE

2.1. Graphene on SiC Substrates

The graphene synthesis is based on the thermal decomposition of SiC at ultrahigh vacuum [2,3]. We used semi-insulating 6H-SiC(0001) substrates. After ex-situ and in-situ cleaning, the sample is annealed at 1700°C for 15 min at ultrahigh vacuum. The C-face plane is used for the device fabrication.

2.2. Graphene on Si Substrates

The concept of the graphene on Si substrates is realized by the epitaxial growth of SiC layer on Si substrates and

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14. ABSTRACT

SiCN deposited by plasma-enhanced chemical vapor deposition (PECVD) using hexamethyldisilazane (HMDS) vapor is studied. During PECVD, hydrogen is used as a carrier gas in addition to HMDS vapor. This becomes an advantage in the graphene process because hydrogen has cleaning effect on graphene surface. To verify this effect, SiCN gate stack is applied to the graphene FETs on SiC substrates. FETs with SiCN gate stack exhibit clearer ambipolar characteristics than FETs with conventional SiN gate stack.

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subsequent thermal decomposition of the SiC surface at the ultrahigh vacuum [4,5]. The SiC layer is grown on Si substrates by gas-source molecular beam epitaxy with monomethylsilane (MMS) gas. After BHF cleaning, the Si substrate is flush annealed at 1200°C at ultrahigh vacuum. Then MMS gas is introduced into the reactor and the pressure is controlled at 3 x 10^{-2} Pa. The growth of SiC layer is carried out at 1050°C for 60 min. The thickness of the SiC layer is 100 nm at this growth condition. Next, the MMS gas is exhausted from the reactor to anneal the sample at 1250°C for 30 min at ultrahigh vacuum. This process forms few layers of graphene on the SiC surface. The formation of graphene is confirmed on Si(100), (110), and (111) substrates [5]. Detailed characterization of graphene on each crystal orientation is reported elsewhere [5]. In this study, we used the graphene on Si(100) substrates for the device fabrication.

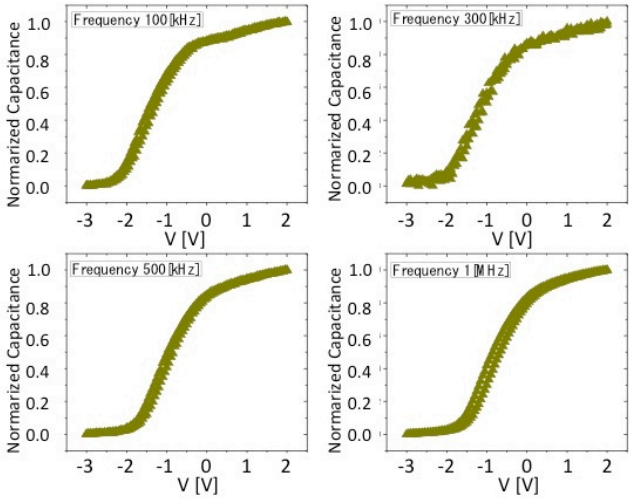

Figure 2. Capacitance versus voltage characteristics of MIS capacitor with SiCN insulator measured at four frequencies (100k, 300k, 500k, and 1MHz).

III. Fabrication Process

Graphene-channel FETs are fabricated both for the samples with SiC substrates and Si substrates. The device fabrication starts with the ohmic metallization. As the ohmic electrodes, Pd/Au (25nm/100nm) is evaporated and lifted off. Next, device isolation is achieved by the oxygen plasma etching of the graphene out of the device area. After depositing dielectric film for the gate stack, Ti/Pt/Au (20nm/20nm/280nm) is evaporated and lifted off for the gate electrodes. Finally, contact holes are opened on the ohmic electrodes, followed by the Ti/Pt/Au metallization for probing pads. The gate length is 3 μm.

For the gate stack, SiCN is deposited by plasma-enhanced chemical vapor deposition (PECVD) using hexamethyl-disilazane (HMDS) vapor [7]. Figure 1 shows the PECVD system. Liquid HMDS is heated at 60°C to vaporize. The HMDS vapor is introduced in the reactor with hydrogen carrier gas. In the gate process, first the sample loaded to the reactor is annealed in pure hydrogen ambient to clean the graphene surface [8]. Then HMDS vapor is introduced in addition to hydrogen with HMDS:H_2 = 1:25. After the pressure is stabilized at 133 Pa, PECVD is carried out at 350°C for 2 min. At these conditions, a 10-nm-thick SiCN is deposited on graphene. The electrical property of SiCN is characterized by capacitance-voltage (C-V) measurements. For this purpose SiCN is deposited on a Si substrate with the same process conditions. Figure 2 shows the C-V characteristics of a metal-insulator-semiconductor (MIS) capacitor consisting of the Ti/Au metal, 10-nm-thick SiCN insulator, and Si substrates. Severe hysteresis is not observed in the frequency range between 100 kHz and 1 MHz. The dielectric constant of SiCN is estimated to be 4.

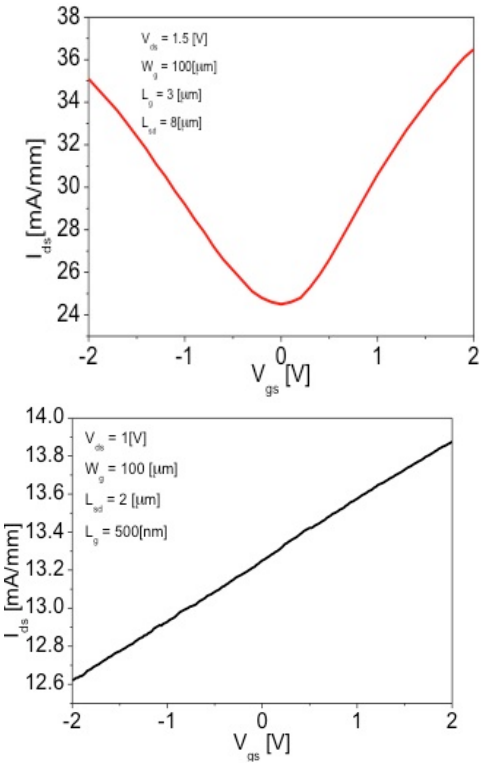

Figure 3. Transistor characteristics of graphene FETs on SiC substrates with SiCN (top) and SiN (bottom) gate stack.

IV. Results and Discussion

4.1. Graphene FETs on SiC substrates

Figure 3 compares the characteristics of 3-μm-gate FETs with the SiCN gate stack and the conventional SiN gate stack. The SiN is deposited by PECVD with monosilane, nitrogen, and ammonia gases. Both samples have graphene on semi-insulating 6H-SiC substrates. The SiCN gate stack exhibits clear hysteresis-free ambipolar characteristics with the channel conduction minimum at zero gate voltage. In contrast, the drain current monotonically increases with the gate voltage for the SiN gate stack in the gate voltage range tested. More negative gate voltage was difficult to try because of a

breakdown of the SiN gate stack. These results indicate that SiCN successfully eliminates the source of the negative shift in the Dirac voltage, such as the interface states and fixed charges in the gate stack.

The maximum transconductance (g_m) of the SiCN gate FET is 35 mS/mm for n-type operation and 33 mS/mm for p-type operation at a drain voltage (V_{ds}) of 1.5 V. The field effect mobility is estimated to be 300 and 280 $cm^2/(V.s)$ for electrons and holes, respectively.

The better FET characteristics achived by the SiCN gate stack is considered as a result of the cleaning effect by hydrogen. It is reported that the hydrogen annealing effectively removes resist scums remaining on graphene [8]. In the deposition of SiCN, hydrogen is used as a carrier gas. This also acts as an *in situ* cleaning of graphene surface that produces better interface between the graphene channel and the SiCN gate stack.

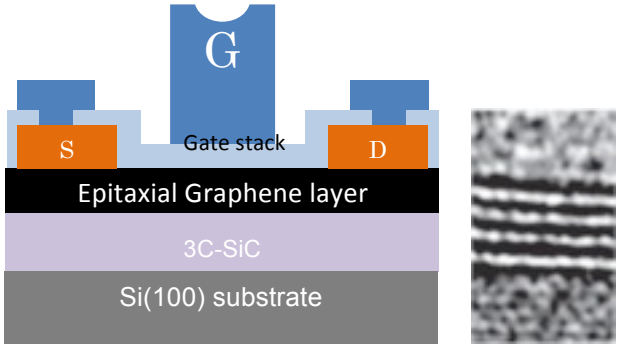

Figure 4. Schematic cross section of GOSFET (left) and TEM image of graphene (right).

4.2. Graphene-on-silicon FETs

Next, the SiCN gate stack is applied to GOSFETs. Figure 4 shows the schematic cross section of GOSFETs and the transmission electron microscope (TEM) image of graphene. Five or six layers of graphene are confirmed. The drain current versus gate voltage characteristics of 3-μm-gate GOSFETs is shown in Fig. 5. Although the shift in the conduction minimum with respect to the gate voltage is observed, the device exhibits clear ambipolar characteristics. The drain current density of GOSFETs is much less than that of the FETs on SiC substrates shown in Fig. 3. This is because of the difference in the graphene quality. However, the GOSFETs with the SiCN gate stack shown in Fig. 5 increases the drain current density by two orders of magnitude comparing to the previously reported GOSFETs with the SiN gate stack (~10^{-3} mA/mm) [6].

V. Conclusion

The SiCN gate stack deposited by PECVD with HMDS vapor improves the transistor characteristics of graphene-channel FETs because of the cleaning effect by hydrogen used as a carrier gas for PECVD. Resulting FETs on SiC substrates exhibit clear ambipolar characteristics with improved transconductance comparing to the previous devices using the SiN gate stack. The graphene-on-silicon FETs with the SiCN gate stack also exhibit clear ambipolar characteristics and larger drain current density than those reported on GOSFETs with conventional SiN gate stack.

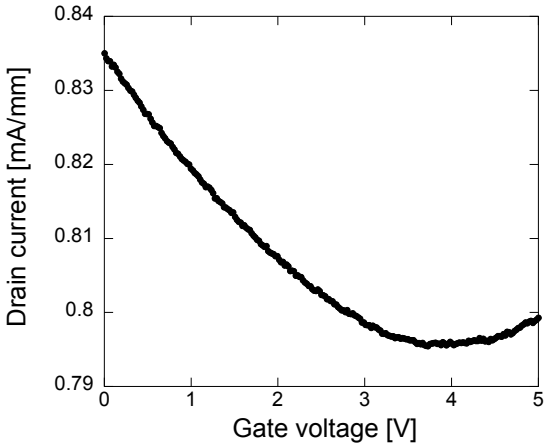

Figure 5. Drain current versus gate voltage of 3-μm-gate GOSFET. Drain voltage is 1 V.

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